

UNITED STATES PATENT APPLICATION

OF

IN DUK SONG

FOR

IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE

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This application claims the benefit of Korean Patent Application No. P00-55034, filed on September 19, 2000, which is hereby incorporated by reference for all purposes as if fully set forth herein.

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## BACKGROUND OF THE INVENTION

**Field of the Invention**

This invention relates to a liquid crystal display device, and more particularly to a liquid crystal display device that is capable of eliminating a stain generated at an outer area of a thin film transistor array using an in-plane switching mode.

## Discussion of the Related Art

Generally, a liquid crystal display of active matrix driving system uses thin film transistors (TFTs) as switching devices to display a natural moving picture. Since such a liquid crystal display can be made into a device that is smaller than a cathode ray tube ("CRT"), it is commercially available for use in monitors such as portable televisions, notebook personal computers and laptop personal computers, etc.

25 etc.

The active matrix liquid crystal display (LCD) displays a picture corresponding to video signals, such as television signals, on a pixel (or picture element) matrix having pixels arranged at each crossing of gate lines and data lines. Each pixel includes a liquid crystal cell for controlling

transmitted light in accordance with a voltage level of a data signal from a data line. The TFT is installed at the crossing point of the gate line and the data line to switch a data signal to be transferred to the liquid crystal cell in  
5 response to a scanning signal (i.e., a gate pulse) from the gate line.

Such a liquid crystal display can be largely classified as twisted nematic (TN) mode, in which a vertical electric field is applied, and an in-plane switching (IPS) mode, in  
10 which a horizontal electric field is applied to have a wide viewing angle. How an LCD is classified depends on the direction of an electric field driving the liquid crystal.

15 The IPS mode LCD has an advantage over the TN mode LCD in that, in an IPS mode LCD, a liquid crystal within a pixel area is rotated in the horizontal direction by a horizontal electric field to have a wide viewing angle.

20 Referring to Fig. 1, the IPS mode LCD includes a TFT 50 provided at a crossing of a data line 52 and a gate line 54, pixel electrodes 48 arranged in a matrix in a cell area between the data line 52 and the gate line 54, and a common electrode 35 formed in parallel to the pixel electrodes 48 in  
25 the pixel area. As shown in Fig. 2, the TFT 50 is provided on a rear substrate 32. The TFT 50 includes a gate electrode 34 connected to the gate line 54, a source electrode 42 connected to the data line 52, a drain electrode 44 connected to the pixel electrode 48, and an active layer 38 defining a channel  
30 between the source electrode 42 and the drain electrode 44.

The gate electrode 34, the gate line 54 and the common electrode 35 are formed by depositing a metal such as chrome (Cr), etc. on the rear substrate 32 and then patterning it. Herein, the common electrode 35 is patterned into a plurality 5 of strips within the pixel area. A gate insulating film 36 made from an inorganic dielectric material such as  $\text{SiN}_x$ , etc. is entirely deposited on the rear substrate 32 provided with the gate electrode 34, the gate line 54 and the common electrode 35. Semiconductor layers consisting of the active 10 layer 38 made from amorphous silicon (a-Si) and an ohmic contact layer 40 made from a-Si doped with  $n^+$  ions are disposed sequentially on the gate insulating film 36. Then, the source electrode 42, the drain electrode 44 and the data line 52 made from a metal material are provided to cover the semiconductor layers 38 and 40. In this case, the source electrode 42 and the drain electrode 44 are patterned in such a manner to be spaced by a predetermined channel width from each other. Thereafter, indium-tin-oxide (ITO) is deposited and then patterned to form the pixel electrode 48. Herein, the 15 pixel electrode 48 is connected to the drain electrode 44 and is patterned into a plurality of strips that partially overlap and alternate with the common electrode 35 within the pixel area. Subsequently, an ohmic contact layer 40 is etched along a channel defined between the source electrode 42 and the 20 drain electrode 44 to expose the active layer 38. A protective film 46 made from  $\text{SiN}_x$  or  $\text{SiO}_x$ , etc. is entirely deposited on the rear substrate 32 to cover and thus protect the TFT 50 and the pixel electrode 48.

As shown in Fig. 3, the rear substrate 32, which is provided with the TFT array, is opposed to a front substrate 72, which is provided with black matrices 74 and color filters



area and the gate link area is coupled with only a gate voltage applied to the gate link 87, via the gate pad 86 upon driving of the LCD to thereby cause deterioration of the liquid crystal.

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More specifically, an electric field corresponding to a voltage difference between a data voltage of the pixel electrode 48 and a common voltage of the common electrode 35 (wherein the pixel electrode 48 is horizontally opposed to the common electrode 35 for each cell) is applied to the liquid crystal 78 of the TFT array 90 when a gate high voltage is applied to the gate electrode 34. Such electric field is maintained during a period when a gate low voltage is applied. By this horizontal electric field, the liquid crystal 78 is driven to control a quantity of a light transmitted from the back light. Generally, a data voltage having the opposite polarity for each successive frame is applied to the liquid crystal 78 to prevent deterioration of the liquid crystal. On the other hand, a gate voltage having the same polarity for each frame is applied to a liquid crystal at the outer area of the TFT array 90, particularly, in the gate link area, for the majority of a frame period. More specifically, a gate high voltage of about +20V is applied to each gate line 54 for a relatively short time during one frame period. A gate low voltage of about -5V is supplied during the remaining portion of the frame period, which is the majority of the frame period. Thus, a gate low voltage having a direct current component is applied to the liquid crystal in the gate link area during the majority of the frame period, thus causing deterioration of the liquid crystal over time. Moreover, liquid crystal deterioration at the gate link area is diffused into the liquid crystal in the vicinity of the edge of the TFT

array 90. As a result, a stain is generated at the periphery of the LCD because of such deterioration of the liquid crystal, thus degrading picture quality and reliability.

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SUMMARY OF THE INVENTION

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Accordingly, the present invention is directed to an in-plane switching mode liquid crystal display device that substantially obviates one or more problems due to the limitations and disadvantages of the related art.

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Accordingly, it is an object of the present invention to provide a liquid crystal display device that is capable of preventing deterioration of liquid crystal at the outer area of an IPS mode TFT array.

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Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

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In order to achieve these and other objects of the invention, an in-plane switching mode liquid crystal display device according to an embodiment of the present invention includes a plurality of data lines for applying data signals to a thin film transistor array; a plurality of gate lines for applying gate signals to the thin film transistor array; a

plurality of gate links extended from the plurality of gate lines into the outer area of the thin film transistor array; and a plurality of common voltage lines, being provided in such a manner to cross the plurality of gate links, to apply a 5 common voltage to the thin film transistor array.

10 These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings.

15 It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

**BRIEF DESCRIPTION OF THE DRAWINGS**

20 The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate 25 embodiments of the invention and, together with the description, serve to explain the principles of the invention.

25 In the drawings:

Fig. 1 is a plan view showing a structure of a conventional IPS mode LCD device;

30 Fig. 2 is a sectional view of the LCD device taken along the B-B' line in Fig. 1;

Fig. 3 is a sectional view representing a driving characteristic of the LCD device shown in Fig. 1;

5 Fig. 4 is a schematic plan view showing an electrode arrangement of the LCD device shown in Fig. 1;

10 Fig. 5 is a plan view showing an electrode arrangement of a LCD device according to an embodiment of the present invention; and

15 Fig. 6 is a driving waveform diagram of voltages applied to the gate line and the common voltage line shown in Fig. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

20 Reference will now be made in detail to the preferred embodiment of the present invention, example of which is illustrated in the accompanying drawings.

25 Referring to Fig. 5, there is shown a liquid crystal display (LCD) device according to an embodiment of the present invention. The LCD devices includes a TFT array 104 for displaying a picture on a rear substrate 100, a plurality of common voltage pads 102 and a plurality of common voltage lines 110 for applying a common voltage from an external driver to the TFT array 104, and a plurality of gate pads 106 and a plurality of gate lines 112.

30 In Fig. 5, the common voltage lines 110 are formed in parallel to the gate lines 112 within the TFT array 104. The

common voltage lines 110 within the TFT array 104 are commonly connected by the common voltage lines 110 crossing the gate links 108 at an outer area of the TFT array 104. In particular, a plurality of common voltage lines 110 also is 5 provided at the outer area of the TFT array 104 to apply a common voltage to a liquid crystal at the outer area thereof. Further, the common voltage lines 110 are connected to the external driver via the common voltage pads 102 formed at the outer area of the TFT array 104. The gate pads 106 connected 10 to the external driver are connected to the gate lines 112 within the TFT array 104 via the gate links 108.

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15 Gate voltages  $V_{gh}$  and  $V_{gl}$  and a common voltage  $V_{com}$  having waveforms as shown in Fig. 6 are applied to the TFT array 104. Referring to Fig. 6, a common voltage  $V_{com}$  of +5V is applied to the common voltage lines 110, while a gate high voltage of about +20V and a gate low voltage  $V_{gl}$  of about -5V are applied to the gate lines 112. The TFTs provided within the TFT array 104 are switched by the gate high voltage applied to the TFT array 104 via the gate pads 106 and the gate links 108 to drive the liquid crystal cells. In this 20 case, the gate low voltage  $V_{gl}$ , which is applied for the majority of the duration period of the gate voltages  $V_{gh}$  and  $V_{gl}$ , is loaded on a liquid crystal at the outer area of the TFT array 104 by the gate links 108 and is distributed and 25 reduced by the common voltage  $V_{com}$  applied to the common voltage lines 110 crossing the gate links 108. The gate voltage applied to a liquid crystal at the gate link area is distributed by the common voltage lines as mentioned above, so 30 that deterioration of liquid crystal can be prevented.

As described above, according to the present invention, a plurality of common voltage lines is provided at the outer area of the TFT array in such a manner to cross the gate links, thereby allowing a gate voltage loaded on a liquid crystal at the gate link area is distributed and reduced by the common voltage. Accordingly, deterioration of liquid crystal caused by the gate voltage at the outer area of the TFT array can be prevent to eliminate a generation of stain.

10 It will be apparent to those of skill in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.